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MODELING OF NBTI DEGRADATION IN P-CHANNEL VDMOSFETs

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This paper gives insight in reliability of p-channel VDMOSFET power transistors subjected to NBT stressing. Effects that lead to degradation of characteristics of these electronic circuits are presented, out of which threshold voltage shift with NBT stressing is further analysed. Measurements have been done and experimental results of the threshold voltage degradation of power transistors IRF9520 caused by different types of negative bias temperature stressing are shown. Stressing types, both static and pulsed, and their impact on transistors, especially on threshold voltage shifts have been explained in more details. An elementary equivalent electrical circuit is designed and proposed with the goal to model impact of both types of stressing, and also to calculate and estimate reliability of the circuit under specified stress. All of the elements of the modeling circuit and their dependencies are explained. Example of modeling from the experimental data is given together with the comparison between measured and modeled results. Differences between obtained results are discussed.

Key words: reliability, VDMOS power transistors, threshold voltage, modeling

INTRODUCTION

In order to provide and maintain certain level of quality control in many different processes, it is needed to insure optimal work of the included electronic devices. One of the on-going questions in electronics is the reliability of the electronic devices. As the downscaling of technology proceeds and with the continuous decrease in devices dimensions, new issues in term of circuits reliability have occured. Possible reliability issues can significantly reduce device operation capabilities and lifetime. Modeling of the reliability of the semiconductors and the effects that degrade devices play a main role for the different factories and integrated devices manufacturers. Therefore, it is needed that reliability problems be considered during the processes of circuit design. One of the most critical limiting factors that determines device lifetime in metal-oxide semiconductor field effect transistors (MOSFET) is negative bias temperature instability (NBTI). This effect is more pronounced with increasing device density. Unpredictability of the NBTI effect has led to the lack of accurate aging models [1].

NBTI has been found to occur mostly in p-channel MOSFETs operated at elevated temperatures (100 - 250˚C) under negative gate oxide fields in the range 2 - 6 MV/cm [1],[2],[3]. Microscopic mechanisms of NBTI are still not well understood, but it is well known that NBTI is manifested as the decrease in device transconductance (g_m) and absolute drain current (I_{Dsat}) and the increase in device threshold voltage (V_T) and absolute “off” current (I_{off}) [2]. Regarding the device parameters, NBT stress-induced threshold voltage shifts are most critical and therefore VT is the most interesting parameter for studying, especially for lifetime estimation [3],[4],[5].

There have been many studies that were conducted to further understand NBTI, and it was reported that this phenomenon is related to the stress-induced generation of oxide-trapped charge (N_{ot}) and interface traps (N_{it}) [2]. Result of these studies was that the role of holes and hydrogen in the degradation process has been identified, and the importance of the concentration of dissociated hydrogen on the defect generation has been declared [2],[3],[4]. Since power MOSFETs are mostly operating at high current and voltage levels that lead to both increased gate oxide fields and selfheating, NBTI has pointed out as one of the critical factor in normal operation of the circuits.

In recent years, there have been many researches with the goal to explore fundamental NBTI mechanisms, with accent in commercially applied MOS transistors and circuits [6],[7]. Some of them were in the direction of finding new and more accurate measuring techniques, and some of them were in the direction of further explaining nature of NBTI effects. It has been shown that NBTI model that describes degradation caused by continual static stress can give wrong reliability presumption in the case of pulsed stressing, which is far more applied. Modeling of pulsed stress degradation remains challenging task, especially because degradation effects depend on both frequency and duty cycle of the stress signal.

Our earlier studies have tackled NBTI effects of p-channel power vertical double diffused MOS (VDMOS) transistors. This type of transistor is suitable device for switching circuits because of its superior switching capabilities, so it is also convinient for pulsed stressing studies. We have investigated reliability of VDMOS devices under various transistor stressing conditions such as high electric field, irradiation and NBTI and irradiation in order to explain both physical and electrical behaviour

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[3],[5],[8],[9],[10]. Modeling of these NBTI effects of p-channel VDMOS transistors presents next incremental step in our research.

EXPERIMENTAL SETUP

In order to obtain appropriate results for threshold shift modeling, experiments have been done on the various groups of the transistors. NBT stressing has been conducted under typical NBTI conditions (voltage of -50 V and temperature of 175˚C) and with different duty cycle of the stressing signal. Main part of the research was on the stressing with stressing signal of duty cycle of 50% (pulse on-time equals pulse off-time), and on stressing with static stress signal.

Samples for this concrete experiment were commercial p-channel VDMOS power transistors IRF9520, which are composed in standard poli-Si gate technology, with hexagonal cell structure (1650 cells) and gate oxide of nominal depth of nearly 100 nm. Maximum drain current of these transistor is 6.8 A, and nominal value of threshold voltage measured before stressing is V_{T0} = -3.6 V. Samples were packed in standard TO-220 package.

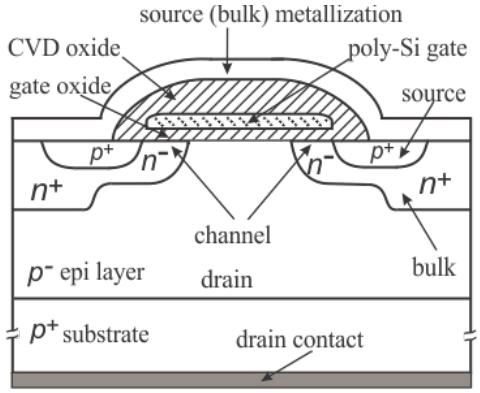

Figure 1: Cross section of two half-cells of p-channel power VDMOS transistor

One group of tested samples was stressed with continuous static signal of V_{stress} = -50 V (while source and drain were grounded). Stressing temperature was 175˚C, and duration of the experiment was 10 hours. On the other hand, other group of tested samples was exposed to identical stressing temperature for the same period of time, but the stressing signal was pulsed. Frequency of the pulsed stressing signal was 10 kHz (period of 100 μs), and the duty cycle was 50%. Results obtained with these experiments are given in the Figure 2.

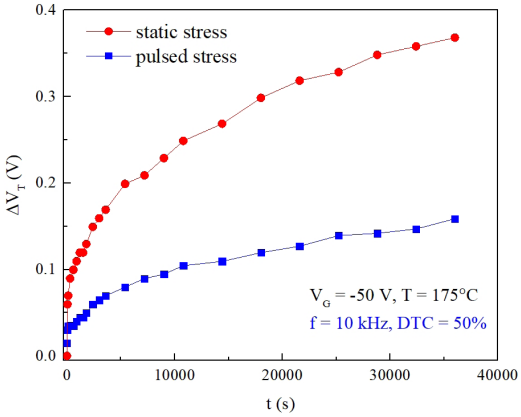

Figure 2: Measured threshold voltage shifts during static and pulsed stress

So far, in almost all of the NBTI effect research, especially in the ones concerning p-channel MOS transistors manufactured in various technologies and regardless of whether the stressing is static or pulsed, results directed to exponential evolution of threshold voltage degradation with time, t^n, where n is less than one (n < 1) [3],[5],[9],[10] Also, obtained results in these experiments, as in the most of others, point out that ΔV_T is significantly greater with static than pulsed stressing.

Additional considerations must be taken in mind during pulsed stress analysis. In order to approach pulsed stress effects appropriately, change of ΔV_T created during single stress impulse, one of the many from the pulsed stress (micro level), must be further explained. On a micro level, evolution of ΔV_T during single pulse can be divided into three parts. First part responds to the on-time of the stressing pulse. During on-time, ΔV_T grows to a certain level. Behavior of the ΔV_T during off-time must be divided, thereby making second and third part of the entire microlevel ΔV_T evolution. During second part (part II in Figure 3), ΔV_T declines to a certain point, partially recovering degradation created during part I. In the third part, there is no change of ΔV_T [9],[10].

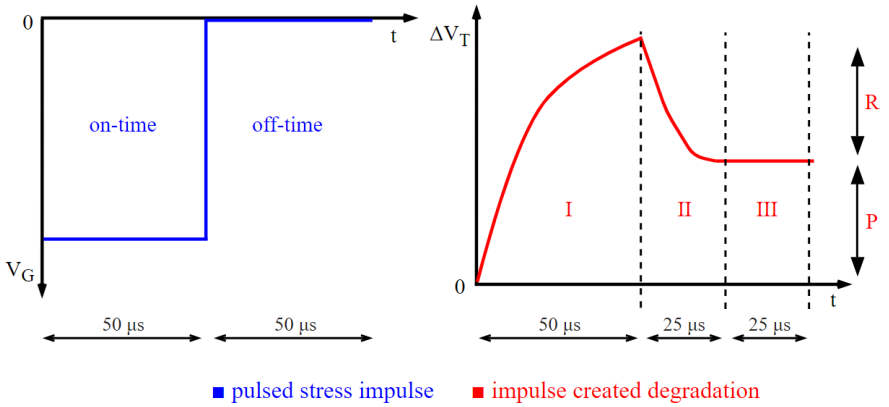

Figure 3: The waveform of stress voltage during the pulsed NBT stress and resulting micro-level signal of ΔV_T (R – recoverable component, P – permanent component)

With these facts, it can be concluded that first part of the evolution presents degradation part, second one recovery part, and the third one constant part. Thereby, value of ΔV_T on a microlevel can be separated into the recoverable component (R) and permanent component (P). Earlier researches have pointed to the existence of a characteristic time constant (25 μs) related to the recoverable and permanent components of stress-induced degradation [6],[7],[9],[10]. It was found that 25 μs off-time of the pulsed stress voltage could suffice to remove the major part of the recoverable component of the degradation created during the foregoing pulse on-time, regardless of pulse duty cycle.

MODELING OF ΔV_T

There were several attempts to model ΔV_T [11],[12],[13],[14]. Important characteristic of modeling circuit is that it should be valid for both static and pulsed stress. Since the evolution of ΔV_T has exponential form, one approach to modeling is that central element of the modeling circuit should be capacitor, because of its exponential response. In this approach, capacitor voltage should be corresponding to ΔV_T. On a micro level, charging of the capacitor presents growth of ΔV_T, while discharging presents decline of ΔV_T. Circuit is further expanded with charging and discharging resistors which will control charging rate of the capacitor, and with some additional elements. Complete modeling circuit is given in the Figure 4.

Resistor R1 is charging resistor that limits and declares charging rate of the capacitor C1. Diode D1 presents ideal diode. Diode should be ideal, because there should be no voltage drop, and it is needed to ensure that capacitor will not discharge through resistor R1 during pulse off-time, when V1 is zero. Discharging part of the circuit is created with serial connection of resistor R2 and JFET (junction field effect transistor) polarized in ohmic region. R2 is discharging resistor which affects discharging of the capacitor, while JFET in ohmic region is used as a voltage-controlled resistor. Resistor RG is the part of the standard ohmic region JFET polarization. Depending of the voltage source V2, JFET J1 can act as a resistor of very small resistance, almost closed switch (which is needed to model pulsed stress), where $R_{J1} << \infty$. Also, J1 can act as a resistor of very high resistance, as open switch (which is needed to model static stress), where $R_{J1} \rightarrow \infty$. Thus, it is possible to consider J1 as a switch which is either closed or open that enables or disables discharging of the capacitor.

For modeling of the static stress, J1 continually acts as a open switch and disables capacitor discharge. Then, modeling of static ΔV_T comes down to mathematcal calculations of particular circuit elements, simple elements of capacitor charging. However, since these types of components are mostly applied in circuits that take advantage of switching characteristics, pulsed stress effects are of greater importance than the effects of the static ones. For modeling of ΔV_T under pulsed stress, during the pulse off-time of the stressing signal period, it is needed that J1 acts as a closed switch, thus enabling capacitor discharge. Since the discharging of the capacitor should be allowed only for a specific time period of 25 μs (between 50 μs and 75 μs of the stressing pulse), during that time, J1 acts as closed switch, enabling capacitor discharge. However, J1 only acts as a closed switch, it still has its resistance R_{J1}. So, the discharging of the capacitor is enabled, but through serial connection of R2 and R_{J1}. For the rest of the period, J1 acts as an open switch, so the discharging of the capacitor is not enabled.

This type of circuit reproduces specific waveform given in Figure 3. Very important aspect of the circuit is that, while J1 acts as the closed switch, resistance R_{J1} varies with the change of V2. With that, eqivalent resistance of the whole discharing part can be varied with the change of magnitude of V2 (as shown in Figure 5). As earlier mentioned, different frequencies and duty cycles of the stressing signal lead to different slopes of the degradation curve. Differents slopes appear because of the different increments on a microlevel per different stressing pulses. With varying of JFET control voltage, given model can adapt to various magnutudes of increments and therefore, cover full scale of either frequencies or duty cycles. Thus, described model can be used to predict reliability of VDMOSFET devices, regardless of the type of the stressing signal.

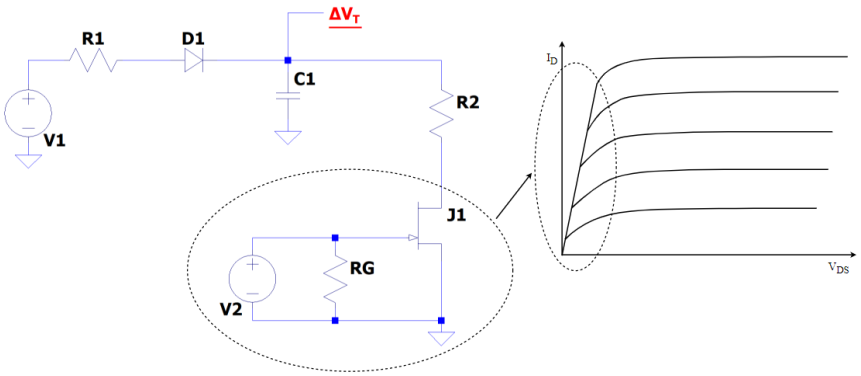

Figure 4: Electrical circuit for NBTI modeling

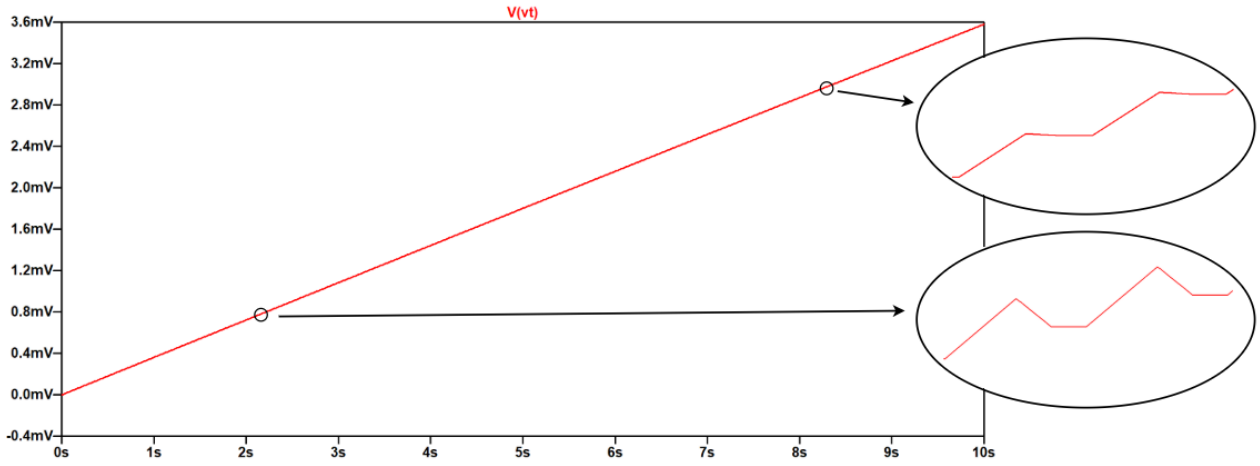

Figure 5: Different types of ΔV_T increment during pulsed stressing

Another phase in modeling is calculating of the values of the elements in modeling circuit, specifically of the capacitor and the resitors. Like in every other modeling problem, there are several ways to approach it. Mostly, it is needed to mark one or two values as constant one, or to compare them to some other physical phenomenons. Since the capacitor is central element, approach is to mark it as constant. Values of R1 and R2 are calculated using Cauchy's integral theorem [15]. As starting values for this calculations, we have used values from some of our earlier models [12],[13],[14]. Modeling results are given in Figure 6.

As can be seen in Figure 6, for the most part of experimental data, modeled results follow measured results. There is a mismatch in the starting parts, but in the later parts those mismatches tend to be minimal. Greater starting mismatch is related to the value of the parameter n that describes evolution of ΔV_T, which is greatest at the start [3],[5]. In the early stress phase, N_{ot} and Nit rapidly increases, but N_{it} saturates faster than N_{ot}. This rapid increase leads to greater ΔV_T in starting stressing phase, but tends to saturate in later phases, creating smaller mismatch. With pulsed stressing, on a microlevel, stress time is shorter (duty cycle 50%), leading to less pronounced growth of N_{ot} and N_{it}, and thereby to smaller mismatch in general. Still, since the model tends to predict devices reliability after reasonable using time, those later parts are of much greater importance for reliability prediction. However, on of the improvement points of the model in general is to expand modeling circuit in order to appropriately describe early stressing phase as well. It is worth mentioning that higher level of match is achieved for ΔV_T under pulsed stress, which is of greater importance of industry appliances.

CONCLUSION

Problem of modeling of NBTI stress induced effects in VDMOS transistors, which is attractive problem in devices quality control and reliability is discussed. Key features of stress induced threshold voltage shifts are explained more in detail. An equivalent electrical circuit for modeling is proposed and on the bases of experimental

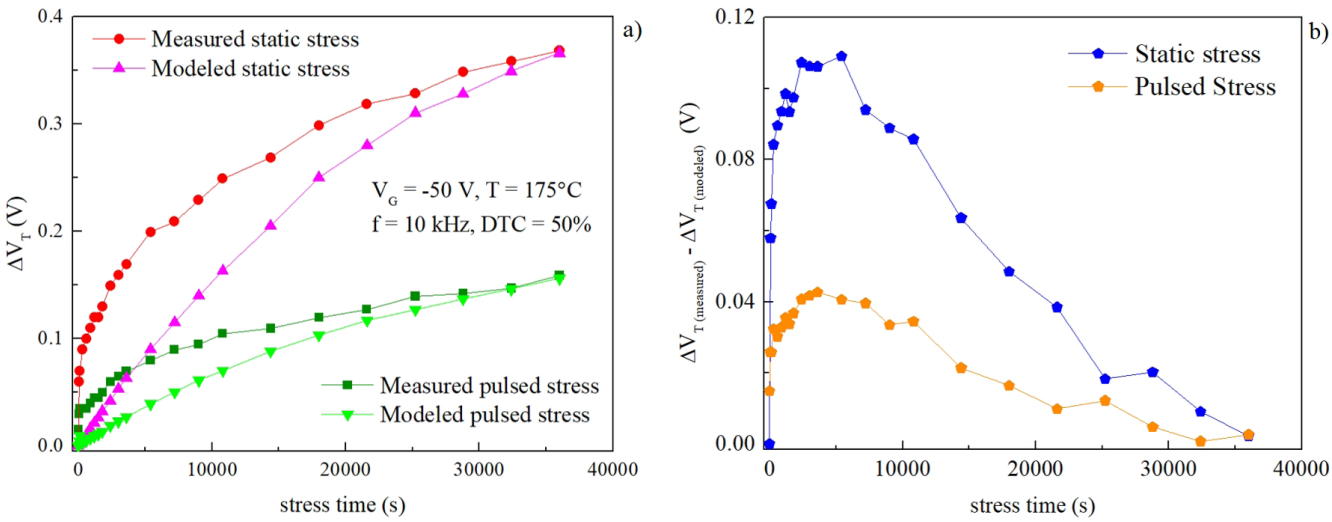

Figure 6: a) Comparison of data obtained by modelling and experimentally b) Deviation of data obtained by measurement and modeling

results, basic modelings of threshold voltage shifts have been carried out. With the use of modeling circuit, high level of matching between measured and modeling results is obtained, except for the modeling of early stressing phases, caused by inital growth of N_{ot} and N_{it}. However, in later phases of stressing, considerably greater matching is achieved, which is of far greater importance in applications. High level of matching of measured and modeled results is especially important in pulsed stress modeling, because VDMOS transistors are widely used in switching circuits. Further development of the proposed model includes analysis of cases where off-time of the pulsed stress signal is shorter than 25 μs, and therefore recoverable component isn't majorly recovered. For that type of stressing, it is needed to expand modeling circuit. Other direction of the future works is deeper mathematical analysis of the problem that leads to the equations that calculate circuit element parameters regardless of fixed values, especially in the part of describing degradation slope.

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