Symbolic Analysis of Faulty Logic Circuits under Correlated Data-Dependent Gate Failures

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Abstract — **In this paper we present a method for symbolic analysis of unreliable logic circuits in the presence of correlated and data-dependent gate failures, described by Markov chains. Furthermore, using this method we investigate the influence of data-dependent failures on the performance of majority logic and multiple input XOR gates.**

Keywords — **Combinatorial circuits, fault-tolerance, Markov chains, symbolic analysis**

I. INTRODUCTION

THE signal probability estimation in digital circuits captures the likelihood of a particular signal being equal to '0' or '1'. The signal probability values indicate how difficult it is to control and test a signal [1]. The problem of signal probability estimation under reliable hardware is analyzed in detail in [2]-[4].

Recently, probabilistic analysis has gained an increased significance in the analysis of unreliable hardware. According to a new design paradigm for very large scale integration technologies, a fully reliable operation is not guaranteed [5]. As the trend of constant decrease of transistors size continues, fault tolerance is recognized as one of the top challenges in semiconductor technology [6]. Increased noise sensitivity is a major drawback of new nano-scale technologies and it is one of the main reasons for so-called transient logic faults. These faults have probabilistic behavior and thus can be described statistically.

Transient faults are usually modeled at logic gates level

and their statistics is given by the probability of an erroneous gate output. If the gate error probability is independent of gate inputs, the model is referred to as *unconditional*. Some methods for unconditional model analysis are presented in [7]-[11]. On the other hand, conditional faults modeling assumes that gate error probability depends on gates input values, as described in [1] and [12]. The state-of-the-art conditional error models analyze only current input values dependence.

In this paper we present a more general fault model that captures the influence of current and previous gate input values on output error probability. Also, based on this error model, a novel symbolic method for faulty gate analysis is described and its application to particular logic gates such as XOR and majority logic is presented.

The rest of the paper is organized as follows. In Section II the previous work related to this topic is presented, which includes the theoretical basis of the faulty gates analysis. In Section III, we present a novel description of faulty gates using Markov chain modeling and a novel symbolic method for gate analysis. Section IV presents the results of probabilistic analysis for some practically significant logic circuits. Finally, some concluding remarks and future research directions are given in Section V.

II. PRIOR WORK

The fundamentals of probabilistic logic circuits analysis are given in [2], where a so-called Parker-McCluskey method for exact signal probabilities calculation was proposed. Based on this method, signal probabilities at the outputs of logic circuit can be determined using individual gates calculation rules. The probability calculation rules for n-input elementary binary logic gates, with inputs x_1, $x_2,…,x_n$ and output z, are given in Table 1, where $p(s)$ denotes the probability that signal s is equal to 1.

TABLE 1: SIGNAL PROBABILITY CALCULATION RULES FOR ELEMENTARY GATES WITH INDEPENDENT INPUTS

Gate type	Probability calculation rule
NOT	$p(z) = p(x)$
AND	$p(z) = \prod_{i=1}^{n} p(x_i)$
NAND	$p(z) = 1 - \prod_{i=1}^{n} p(x_i)$
OR	$p(z) = 1 - \prod_{i=1}^{n} (1 - p(x_i))$
NOR	$p(z) = 1 - \prod_{i=1}^{n} p(x_i)$

The Parker-McCluskey algorithm calculates the signal

probabilities at the output of every individual logic gate g in an m-input circuit C in terms of primary input signal probabilities of C. If the inputs of g are not independently controllable from the primary inputs of C, signal probability at the gate output cannot be determined using Table 1. Instead, the output signal probability $p(z)$, can be expressed in terms of $p(x_1)$, $p(x_2)$, ..., $p(x_m)$, where x_i, $1 \le i \le m$, represents the i-th primary input. The method states that if we first express $p'(z)$, the probability of the gate output signal assuming input independence, $p(z)$ can be derived by suppressing all exponents $(p(x_i))^j$, $j > 1$, $1 \le i \le m$, in a given expression as follows

$$p(z) = p'(z)\big|_{(p(x_i))^j = p(x_i),\ j>1, 1 \le i \le m} . \qquad (1)$$

Although the presented algorithm originally considered only perfect gates, it can easily be expanded for faulty gate analysis if gate failures are modeled as unconditional.

The most common way for analyzing the faulty gates is the so-called mutant modeling approach. According to this approach every 2-input gate in a circuit is substituted with its faulty "mutant", a gate with an equivalent Boolean function whose output is sometimes incorrect.

The correct binary output value of a given gate, $z_c(k)$ at discrete time k, $(k>0)$, depends on the gate binary input values, denoted by $x_1(k)$ and $x_2(k)$. This is illustrated in Fig. 1. Faults are inserted at the gate output by performing XOR operation between a correct gate output sequence $\{z_c(k)\}_{k>0}$, and an error sequence $\{e(k)\}_{k>0}$, producing the actual output sequence $\{z_e(k)\}_{k>0}$. The error sequence $\{e(k)\}_{k>0}$, represents the binary time series which describes the statistics of faults. If the k-th value of error pattern is '1', i.e. $e(k) = 1$ $(k > 0)$, the output of a 'mutant' gate at time k will be faulty.
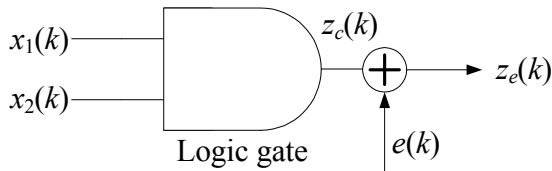

Fig. 1. Faulty gate modelling using "mutant" approach.

The assumption that the probability of faulty output $p(e)$ is independent of gate's input values corresponds to an unconditional error model. It is obvious that in this analysis an error pattern can be treated as a common primary input, with signal probability $p(e)$. Thus, the Parker-McCluskey algorithm can be used for output signal probability calculation.

There are also several other algorithms that use independent fault modeling, including Probabilistic Decision Diagrams (PDDs), Four-Event (FE) Trigonometric Probability Calculation (TPC), Reliability Analysis Logic Failures (RALF) algorithm and Boolean difference calculus.

The PDD algorithm uses directed acyclic graphs to describe the error probability of an individual gate [7]. When all gates PDDs are formed, they are recursively merged from inputs to outputs. The FE method describes signal behavior using four different states: 1, 0, e and e', where e and e' represent an erroneous value and its

negation, respectively [8]. Algorithm calculates the probability that a faulty value, originating from a particular gate g, will be observed at a circuit output. According to TCP approach, every signal distribution probability is represented as an angle and an error probability as its linear rotation [9]. By using trigonometric calculation, output probability is determined. RALF algorithm can be used for reliability calculation of a circuit given in the deterministic decomposable negation normal form [10]. Boolean difference calculus is used in [11] for modeling error propagation from circuits inputs to outputs.

More realistic fault models take into account existing data-dependence of gate error probability and are referred to as *conditional*. The two well known representatives of this class of methods use Bayesian network [12] and Probabilistic Transfer Matrix (PTM) approach [1], respectively. In both methods, erroneous value appearance depends on the gate input values. However, both algorithms consider that only current input values influence the error occurrence. In the next section we present a more general modeling approach which depicts the influence of current and previous gate input values.

III. SYMBOLIC ANALYSIS OF FAULTY LOGIC GATES

A. Fault modeling using Markov chains

In contrast to the state-of-the-art modeling of faulty gates that considers only the failure dependence on current input values, our model captures more accurately the correlation influence by using Markov chains.

Consider a 2-input binary logic gate. In the model the error value at k-th time point $e(k)$ is formed based on a pair of current and M-1 pairs of prior consecutive input values $x_1(k)$, $x_2(k)$, $x_1(k-1)$, $x_2(k-1)$..., $x_1(k-M+1)$, $x_2(k-M+1)$). Let S be a Markov source generating the error sequence composed of 2^{2M} states s_i, $1 \le i \le 2^{2M}$, i.e. $S = \{s_1, s_2, ..., s_{2^{2M}}\}$. Every state corresponds to one possible binary sequence of length $2M$, $s_i = [b_1 \quad b_2 \quad ... \quad b_M b_{M+1} \quad b_{M+2} \quad ... \quad b_{2M}]$, $b_j \epsilon \{0,1\}$, $1 \le j \le 2M$, $1 \le i \le 2^{2M}$, where the first M bits represent the consecutive values of input x_1 and the second M bits represent the values of x_2. Every state can capture the different data-dependent failures, expressed through different error probabilities $P_e(s_i) = \Pr\{e(k) = 1 \mid s_i\}$, $1 \le i \le 2^{2M}$, $k>0$, where $\Pr\{.\}$ denotes probability.

The relations between error probabilities in different states depend on a specific gate. For example, at the output of NAND logic gate a correct value '1' appears only if both inputs are equal to '0'. Thus, if one input changes its value due to an increased noise level, the gate output will be faulty. Consequently, the all-zero state has the highest and the all-ones state has the lowest error probability. For any other state we form a simple model in which the number of ones in the state binary representation (the state weight) determines the error probability. The last conclusion can be formulated as follows

$$P_e(s_i) = \Pr\{e = 1 \mid s_i\} = A_i \Pr\{e = 1 \mid s_0\}, \quad 1 \le i \le 2^{2M}, \quad (2)$$

where A_i represent the scaling coefficients, dependent on

state s_i. From the discussion presented above it holds

$$A_i = 1 / p^{w(i)},\ p \ge 1, \qquad (3)$$

where $w(i)$ denotes the weight of state s_i. The parameter p enables us to change easily the values of scaling coefficients and model different fault conditions. A similar analysis can be performed for other elementary logic gates.

B. A novel approach for faulty gate analysis

We next present a novel symbolic algorithm for faulty gates analysis which combines the Parker-McCluskey algorithm with the data-dependent failure model given in the previous subsection.

The probability that a signal value at the output of a 2-input faulty logic gate is equal to '1'can be expressed as

$$
P_{out} = \sum_{i=1}^{N} p_1^{w_1(i)} \left(1-p_1\right)^{M-w_1(i)} p_2^{w_2(i)} \left(1-p_2\right)^{M-w_2(i)} P_e\left(s_i\right)
$$
$$
+ \sum_{i=N+1}^{2^M} p_1^{w_1(i)} \left(1-p_1\right)^{M-w_1(i)} p_2^{w_2(i)} \left(1-p_2\right)^{M-w_2(i)} \left(1-P_e\left(s_i\right)\right), \qquad (4)
$$

where p_1 and p_2 denote probabilities that a value '1' appears at the gate inputs x_1 and x_2, respectively, while $w_1(i)$ and $w_2(i)$ represent, respectively, the weight of the first and second M bits in a binary representation of state s_i, $1 \le i \le 2^{2M}$, and N denotes the number of states of Markov source S in which a correct output value is equal to '0'.

The expression contains the exponents of input probabilities which appear as a consequence of the multiple discrete times analysis. It is obvious that suppressing them, as stated in the original Parker-McCluskey algorithm, does not lead to a correct result. To distinguish exponents originated from different time points from exponents that appear because of signal space correlation, we present a variable substitution method. The variable p_k $(k = 1, 2)$ from Eq. 4 is substituted with M variables $p_{k,n}$, $1 \le n \le M$, and we have

$$
P_{out} = \sum_{i=1}^{N} \prod_{j=1}^{M} p_{1,j}^{s_i(j)} \left(1-p_{1,j}\right)^{\overline{s_i}(j)} \prod_{j=M+1}^{2M} p_{2,j}^{s_i(j)} \left(1-p_{2,j}\right)^{\overline{s_i}(j)} P_e\left(s_i\right)
$$
$$
+ \sum_{i=N+1}^{2^{2M}} \prod_{j=1}^{M} p_{1,j}^{s_i(j)} \left(1-p_{1,j}\right)^{\overline{s_i}(j)} \prod_{j=M+1}^{2M} p_{2,j}^{s_i(j)} \left(1-p_{2,j}\right)^{\overline{s_i}(j)} \left(1-P_e\left(s_i\right)\right), \qquad (5)
$$

where $\overline{s_i}(j)$, $1 \le j \le 2M$, $1 \le i \le 2^{2M}$, represents a complementary value of $s_i(j)$.
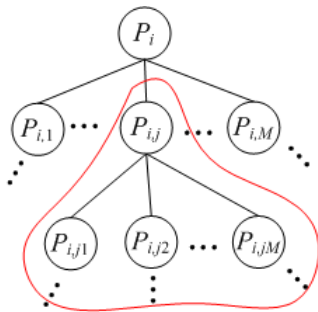

Fig. 2. Illustration of variables substitution method.

If substitution is carried out for every input probability, through every signal path in an m-input circuit, all exponents in the expression for circuit output signals probabilities result from signals space correlation. The

variable substitution is performed by parent-children principle – at every level of substitution a parent variable is substituted with M children variables, as illustrated in Fig. 2. Then the Parker-McCluskey method can be applied for suppressing exponents. At the end all variables are turned back into starting variables p_1, p_2, ..., p_m and the exact expressions for circuit output probabilities are derived.
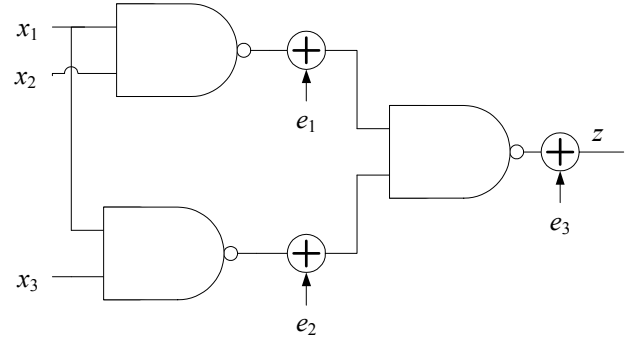

Fig. 3. 3-input test bench for symbolic algorithm validation.

It can be noticed that error probabilities also propagate similarly as primary input probabilities. In order to analyze signal space correlation accurately, the error probabilities of every logic gate must be labeled differently and treated by the Parker-McCluskey method.

The presented algorithm is validated using 3-input test bench shown in Fig. 3. The input denoted as x_3 propagates through a reconvergent fanout creating two correlated signal paths.
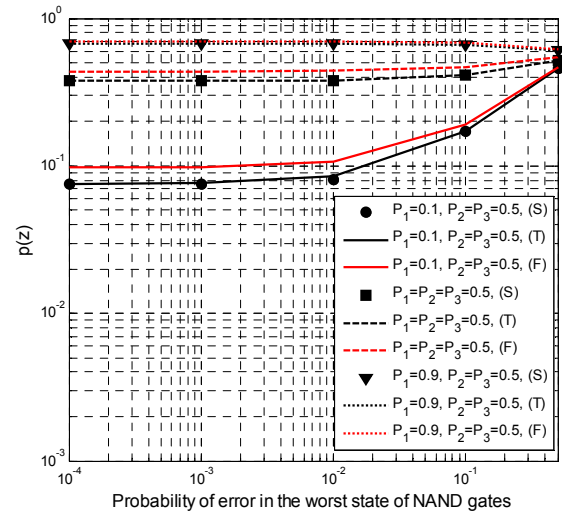

Fig. 4. Signal statistics at the output of test bench given by Fig. 3.

Statistics of circuit output signal, $p(z)$, for different values of input probabilities, $P_1 = p(x_1)$, $P_2 = p(x_2)$ and $P_3 = p(x_3)$ are presented in Fig. 4. It is assumed that every component gate failures are modeled using identical Markov chains. All results obtained using the presented method (denoted by (T)) are validated by Monte Carlo simulation results (denoted by (S)). Results obtained when all paths in the circuits are considered spatially uncorrelated and exponent suppressions are not performed,

are also presented in the figure (denoted by (F)). They do not adequately represent output signal probabilities and are especially inadequate in the region with low gate failure rates.
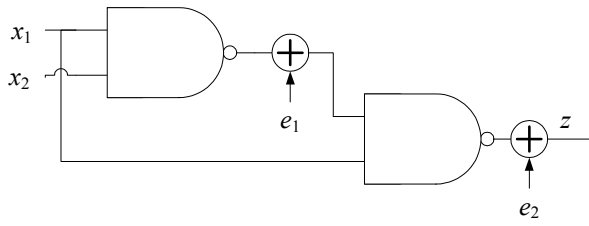

Fig. 5. 2-input test bench for symbolic algorithm validation.

It can be noticed that due to asymmetric paths in the circuit, the variables from different levels of substitution may appear in final expressions. A parent variable influences each children variable (originated from that parent) when multiplied with the children variable, needs to be suppressed. For example, the factor $p_i \cdot p_j \cdot p_{i,1} \cdot p_{i,11}$ reduces to $p_i \cdot p_j$.

To test this part of the substitution algorithm we use a simple 2-input test bench shown in Fig. 5. Output signal probabilities for different worst case failure rates of component NAND gates and different input signal statistics are presented in Fig. 6. Results obtained using a symbolic algorithm (denoted by (T)) match perfectly with the values obtained by Monte Carlo simulation (denoted by (S)).

C. Complexity analysis

We next present the complexity analysis in terms of the number of variables needed for symbolic calculation. The number of variables depends on the number of circuit inputs and length of paths that are affected by signal correlation. Let C be a logic circuit, with m inputs, k of which are spatially correlated ($k<m$). The set of correlated input signal can be denoted as $S_k = \{x_1, x_2, \dots x_k\}$. The remaining $m\text{-}k$ circuit inputs do not produce exponents in output probability expressions and there is no need to substitute their probability variables.

Let N_i be the number of correlated signal paths with different lengths that involve the input x_i, $1 \leq i \leq k$. Let $D_i^{(j)}$, $1 \leq j \leq N_i$, $1 \leq i \leq k$, represents the length of the j-th correlated path in which the input x_i is involved. Then, the total number of variables used can be expressed as follows

$$N_{tot} = m - k + \sum_{i=1}^{k}\sum_{j=1}^{N_i} M^{D_i^{(j)}}. \qquad (6)$$

It can be noted that even for a small number M, the number of variables can be large if long correlation paths exist in a circuit. Symbolic calculation with a large number of variables can be time-consuming, which makes the presented algorithm impractical for the analysis of large logic circuits.

IV. APPLICATION TO ML AND XOR CIRCUITS ANALYSIS

We next present the results for m-input majority logic (ML) and XOR gates analysis built only from faulty 2-input NAND logic gates. Faults are modeled by Markov chains and the probabilities of erroneous circuits outputs

are calculated using the presented algorithm.

All graphical results are obtained assuming that error occurrence at the output of faulty NAND gate depends on two consecutive input values, which corresponds to $M = 2$.

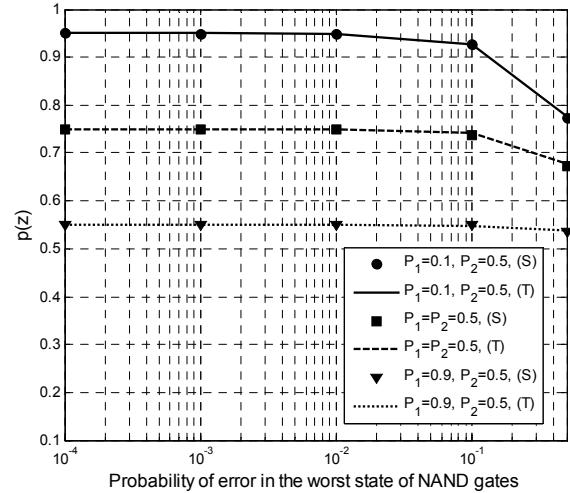
Fig. 6. Signal statistics at the output of test bench given by Fig. 5.

Also, for every m-input circuit the same statistics is assumed for every input and described by probability that input values x_i, $1 \leq i \leq m$, are equal to '1', denoted as P_1.
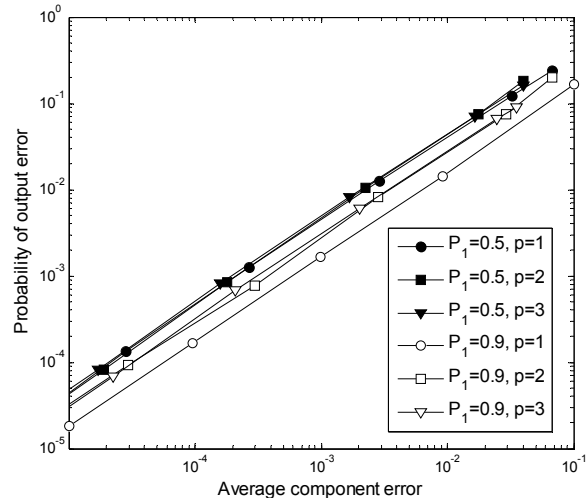

Fig. 7. Probability of error at the output of 3-input ML logic gate.

The output error probability of 3-input ML gate dependence of average component failures is presented in Fig. 7, for several values of parameter p (=1, 2, 3) and two input probabilities $P_1 = 0.5$ and $P_1 = 0.9$. A majority logic gate output is equal to '1', if half or more inputs are equal to '1'. Thus, when ones and zeros appear at the gate inputs with equal probabilities ($P_1 = 0.5$) more gate output values will be faulty, compared to a case when almost all inputs are '1' ($P_1 = 0.9$). When $P_1 = 0.5$, the parameter p, which describes the presented Markov model, does not have any impact on the circuit performance, while the performances differ when $P_1 = 0.9$. The performance comparison of ML gates with different number of inputs is presented in Fig.

8, when $p = 2$. It can be noted that the 2-input majority logic gate has the lowest output error probability when $P_1 = 0.5$. However, when $P_1 = 0.9$, the gate with the largest number of inputs (4-input gate) outperforms other logic gates.

The data-dependence does not influence greatly the probability of error at the output of 3-input XOR gate, as illustrated in Fig. 9. This phenomenon is a consequence of the more symmetric circuit topology in which all error states are approximately equally likely.

Performances of XOR gates with 3, 4 and 5 inputs are presented in Fig 10. It can be noted that increasing the number of inputs causes a higher output error probability. In an XOR logic circuit with more inputs, there are more gate failure combinations that may generate an output error.
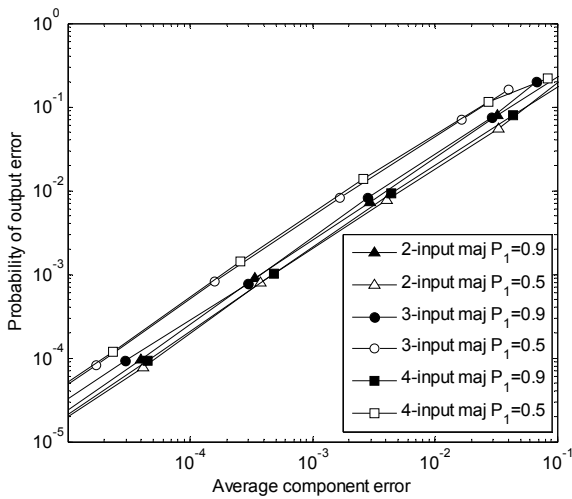

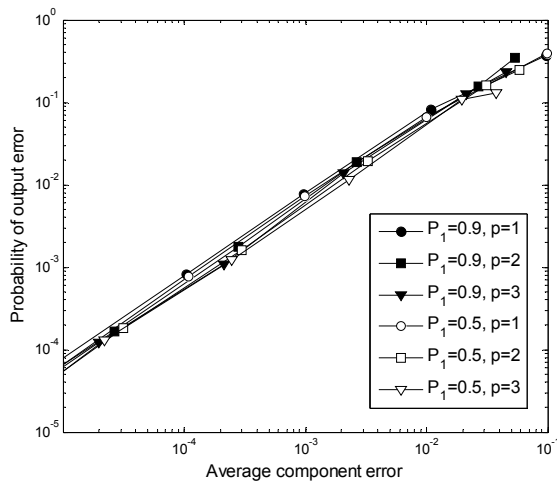Fig. 8. Comparison of majority logic gates with different number of inputs for p=2.

Fig. 9. Probability of error at the output of 3-input XOR logic gate.

V. CONCLUSION

In this paper we have presented a novel approach for transient faults modeling and analysis in combinatorial logic circuits. Using Markov chains, the error sequences at the output of a logic gate can be described in a more general way compared to the existing models.

Our future research is directed to ensuring fault-tolerance in digital networks, built from unreliable components. We are especially investigating memory architectures that use low density parity check error correcting codes. Presented algorithm can be used for the analysis of state-of-the-art memory architectures and under more realistic gate failure scenarios and designing novel architectures that are resistant to correlated data-dependent gate failures.
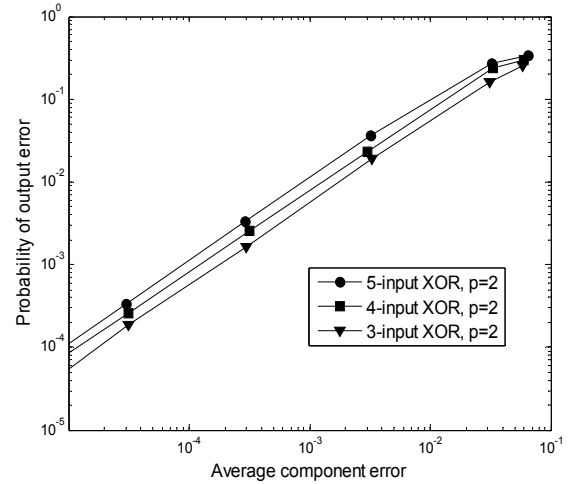

Fig. 10. Comparison of XOR logic gates with different number of inputs.

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