



AN EXAMPLE OF VHF RADAR SIGNAL PROCESSING

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Abstract: Track While Scan (TWS) radars are generally used in defense systems, which supervise the positions of the target and generate the measurements, scan by scan. They measure a target's coordinates, determine its trajectory, and predict its next location. The selection and adaptation of the technical requirements of the optimal hardware for processing and displaying the radar image is related to several serious challenges, such as the availability and price of components on the market, the type of modulation, frequency agility, shielding from interference, computational complexity of processing, type and technology of the antenna system. In the paper, a complete example of coherent hardware processing (reception and transmission) of signals for VHF band radar is proposed. The proposed hardware generates trigger signals, modulates the transmit signal, transmits via a semiconductor HPA transmitter and then at the reception receives signals in the analog domain, converts them, processes them and displays the radar image on the monitor. The numerical experiments have shown the possibility of signal processing in real time on the selected platform showed the justification of the application.

Keywords: digital signal processing, doppler radar FPGA platform.

1. INTRODUCTION

Very High Frequency (VHF) radar techniques are easy to employ and commonly used in defense applications. Fast algorithms and powerful processors facilitate the development of several kinds of low power radars, but the reduction of the transmitted power has to be compensated by on-line processing of an encoded signal to maintain a favorable signal-to-noise ratio suitable for detection. Moreover, radars have to reconstruct return echoes with different travel times due to various origins (multi-path, adjacent objects, etc.) [1]. Such needs can be accomplished by means of signal phase coding and one of the most attractive is the reversal phase code. The composite echo signal must be processed to extract the physical information useful for the measurement considered. In this paper some algorithms used for on-line processing of phase-coded signals will be described, both in time and frequency domain. The trend in VHF radars is to simplify the system hardware, reduce transmitted power and develop more powerful techniques of signal processing. With the advent of powerful Digital Signal Processors (DSPs) and very fast PCs, the implementation

of these algorithms, that give to VHF radar systems the required performances, has become possible [2]. Although these algorithms can be implemented both in time and in frequency domain, working in frequency domain has given faster and more powerful results. The essential first step is the quadrature sampling and the Analog-to-Digital (A/D) conversion. The information is available in digital format, ready for the actual processing carried out in the second step. The quadrature sampling allows all the information included in the received signal to be captured for subsequent processing. These two passages are essential for the following detection process, to extract relevant information from the received echo (i.e. position, velocity, reflected energy, etc.). The third step is the operations on the processed signal, such as data display or data storage for further analysis (off-line), worked out by a PC. Nonetheless, in frequency domain new processing techniques are possible, so such an approach has become dominant [3].

The first step is usually implemented by a digital circuitry, which follows an analog receiver providing an amplification and filtering of the received echo (radio frequency). In some cases a good design of the receiver can limit the amount of noise entering the system: the

noise produced inside the receiver itself (thermal, due to images, etc.) and those coming from the environment that are not exactly inside the frequency band used by the radar system. In other cases it is difficult to discard such external noise, so different methods must be applied to increase the Signal-to-Noise ratio (S/N); they are implemented subsequently. The signal processing is usually done by a specific DSP, but, because of the calculation power of modern PCs, could be carried also on a general purpose computer [4].

Paper is organized as follows: at Section 2, a basic problem statement is given. Section 3 contains description of main radar processing. In Section 4 the results of experiments are given and in Section 5 the concluding remarks presented.

2. PROBLEM STATEMENT

The modern radar use pulse compression, that is to say we spread the transmitted pulse out in time and then process the received echo with a matched filter to de-spread it. The band-limit also return and demodulate radar signal to a complex base band. Also, we measure the echo power and the Doppler shift between successive echoes to obtain the desired measurements. The radar echo pulse demodulated and digitized into a number of complex samples. Each sample index corresponds to a specific time offset from the start of the radar pulse, so each sample represents the reflected energy at a specific range. The complex time series of samples at a given range gate can be processed with a Fourier transform to obtain the Doppler spectrum of the echo at that range, from which the mean velocity and variance can be obtained. For a pulsed radar, it can be shown that the pulse pair algorithm provides a reliable estimate of the mean Doppler frequency at each range gate:

$$R = \frac{1}{N} \sum_{k=0}^{N-1} S_{k+1} S_k^* \quad (1)$$

where S_k are successive samples at a range gate, * indicates the complex conjugate and N is number of samples. We compute the average power along with the mean Doppler shift to provide a reference and for measuring the total area of the raindrops at a given altitude. The average power at each range is:

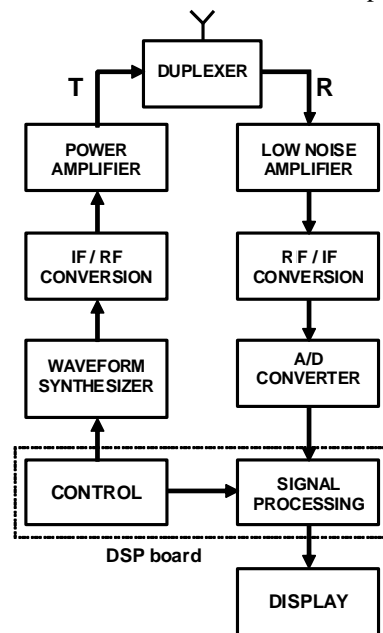
$$R = \frac{1}{N} \sum_{k=0}^{N-1} \text{Re}\{S_{k+1} S_k^*\} \quad (2)$$

We can transmit a long coded pulse, and then compress the echo into an impulse in the receiver using a matched filter. The idea is to spread the transmitted energy out over time to limit the peak transmitted power, then use correlation at the receiver to recover the range resolution. In our case, the coded transmit pulse is a linearly swept frequency 'chirp'. The transmitted pulse can be viewed as a convolution of an impulse and a filter with an impulse response equal to the desired transmitted waveform.

3. RADAR SIGNAL PROCESSING DESCRIPTION

3.1 Concept of Software Defined Radar

The scheme of software radar is shown in Pic.1. Each block consists of modular components, so it is possible to combine components, in order to achieve the desired function. The block waveform synthesizer generates an appropriate transmitted signal of a pulse or continuum nature that will modulate the hyper frequency carrier. He is flexible, which means that the transmitted signal shape can be changed during operation. For radars working with signals in an spread spectrum, the wavelength synthesizer generates a forward signal that is encoded by frequency or phase, which contributes to improved resolution at a distance. The IF/RF conversion block, the spectrum of the generated signal should be transmitted to the hyper-frequency range of the gigahertz level. On the basis of software radar concept we realized functional model of software radar receiver (SRR) from A/D converter to display [5]. After IQ demodulator follows A/D (Analog to Digital) converter and then follow blocks PXI platform.



Picture 1. Software defined radar system

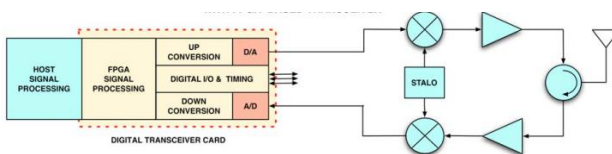
3.2. Design of Solid State VHF transceiver

Higher transmitted power was obtain by combining multiple amplifiers in parallel. In general power amplifier (PA) design theory, the method of using a conjugate match of the external networks connected to the input and output of the transistor devices, would seem to suffice. In practical situations this does not take into account the limitations of the devices. This paper aims to investigate the development of four separate VHF-Band radar HPA moduls using commonly available transistor. The moduls would be combined in paralel design in order to provide a high output power. In the investigation of these developments, certain aims need to be considered. Firstly, and most importantly for radar HPA design, is the available output power. It was decided that the designs

should, at least, meet the specified output power of the device being used. Secondly, the amplifiers should provide this output power over the specified bandwidth. Typical layout of a proposed cascaded power amplifier system has driver amplifiers, main power amplifiers as well as splitters, combiners, circulators and high power terminations. In our design there are no high power circulators and terminations. The input divider for four modules is standard Wilkins divider realized in microstrip. The output combiner is reflective four input type realized in the microstrip. It consists of 25Ω quarter of lambda transformer. The parallel work of two symmetrical transistors on the same device is allowed by the push pull configuration. There are two BALUNs: one at input and other at output. The BALUNs are original; in the technique of symmetrical microstrip. The BALUN is divider and the matching network at the same time. The RF switch is RSW-2-25P with the switch time of 10ns. During the receive time, the power amplifier must be turned off. In order to get fast switching on, the bias of MOSFET must be done prior to RF input signal.

3.3. Example of general purpose FPGA for Radar Controller and Signal Processor

The FPGA provides the computational foundation for a radar controller and signal processor, but it must be integrated with other hardware. A transceiver card is required which can provide receive, transmit and control signal functions. Commercial vendors provide products that provide this general-purpose functionality. The FPGA is typically combined with analog-to-digital and digital-to-analog converters, local memory, digital I/O lines and bus interfaces (Pic.2). The Pentek Model 7142 (Pic. 3) has compact card which is based on the Portable Mezzanine Card (PMC) format. A wide variety of carrier cards are available to host the PMC in common computer backplanes. The hardware vendor typically offers a board support package, which provides drivers and application libraries for the host system, and firmware source code for the FPGA. The first two provide facilities to access the card on various operating systems. The firmware package can be a version of VHDL code that will run on the FPGA and provide baseline functionality, so that the card can be used in some cases without any VHDL development. The end user can customize the supplied VHDL for their specific purposes.



Picture 2. Schematics of a radar system with FPGA transceiver.

The dashed line boxes denote functions that are performed by the FPGA firmware. The FPGA integrated circuit is enclosed within the heat sink.



Picture 3: The Pentek 7142 FPGA transceiver.

3.4. Matched filtering

The impulse response of a matched filter is defined by the particular signal to which the filter is matched. Matching will result in the maximum attainable SNR at the output of the filter when signal, to which filter it was matched, to which it was added white noise, are passed through it. In radar applications, SNR is of paramount importance, and matched filters are used extensively. The probability of detection is related to the SNR rather than to the exact waveform of the signal received. The input to the matched filter is the signal $s(t)$ and additive white Gaussian noise with a two-sided power spectral density of $N_0/2$. Obtaining of the impulse response $h(t)$ that will yield the maximum output SNR at a predetermined delay t_0 was explained in [6]. We look for the response $h(t)$ that will maximize SNR:

$$\left(\frac{S}{N}\right)_{out} = \frac{|s_0(t_0)|^2}{n_0^2(t)} \tag{3}$$

Let the Fourier transform of $s(t)$ be $S(\omega)$, then the output signal at t_0 is given by:

$$s_0(t_0) = \frac{1}{2\pi} \int_{-\infty}^{\infty} H(\omega) \cdot S(\omega) \exp(j\omega t_0) d\omega \tag{4}$$

The mean-squared value of the noise, which is independent of t is:

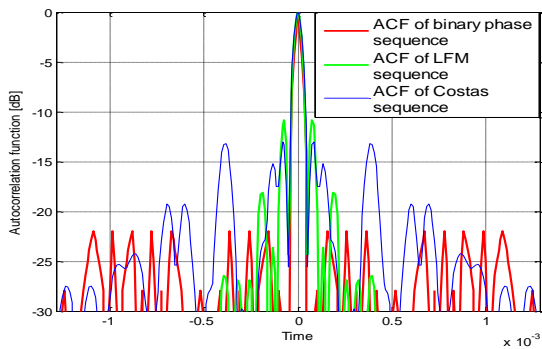
$$\overline{n_0^2(t)} = \frac{N_0}{4\pi} \int_{-\infty}^{\infty} |H(\omega)|^2 d\omega \tag{5}$$

After adding the values (3) in (2), and after the execution explained in [6], the maximum output SNR it was obtained when:

$$H(\omega) = K \cdot S^* \exp(-j\omega t_0) \tag{6}$$

In [6] it was derived that maximum SNR is $2E/N_0$. The impulse response is linearly related to the time-inverted complex-conjugate signal, which represents autocorrelation function (ACF). When the input to the matched filter is the correct signal plus white noise, the peak output response is related to the signal's energy.

In order to emphasize peak-side lobe ratio of sequences used in this paper, its ACF will be presented in decibels.



Picture 4. ACF of used radar sequences

Pic. 4 shows that the best peak-side lobe ratio is obtained using binary phase sequence with 25 elements, and amounts of 22 dB. Besides that it is important to note, that binary phase sequence has the same level of all side lobes, unlike other two sequences.

4. SIMULATION RESULTS

4.1. FPGA Zedboard

The FPGA ZedBoard, which was used in this paper, represents Zynq-7000 FPGA (Pic. 5) evaluation and development kit, and it is equipped with the reconfigurable devices. Zynq system on the chip (SoC) integrates a Xilinx 7-series FPGA and ARM Cortex-A9 dual core based processor system on same chip together. ZedBoard has coherent multiprocessor support, three watchdog timers, one global timer, and two triple-timer counters. In Zynq-7000 FPGA the parts containing intense computations are performed on FPGA. The control parts not containing computations can be done on the processor by using software.



Picture 5. The FPGA Zedboard

Hardware platform configuration for Zynq device consists of two parts: Processing System and Programmable Logic with 85000 cells. The intercommunication between two different portions of electronic circuits is described as Programmable Logic. The upper basic portion, called the processing system (PS), works like a traditional processor. It is mainly formed by the ARM Cortex-A9, DDR3 controller for external DDR3_SDRAM memory and UART for serial communication. Programmable logic

part contains the structures of standard FPGA [5]. Because the FPGA Zedboard performs signal processing in digital form, it was necessary to perform digital to analog conversion for displaying of obtained signal [7]. For that operation the two-channel 12-bit D/A converter Pmod DA2 was applied, which was connected on six-pins PMOD connector JB. It is important that the sampling rate of this D/A converter is 16.5 Mega Sample, and that represents the limitation for displaying short signals with high sampling frequency, such as radar signals. In order to observe generating and processing of obtained signals, the instrument Analog Discovery in oscilloscope mode was used [8]. Using DIGILENT's software for this instrument it was possible to record results of matched filtering and compare it with results obtained in program MATLAB.

4.2. Development of a digital platform

As part of the continuation, it is necessary to define and test the effectiveness of suitable synchronization impulse waveforms as well as types of modulations for use in the test piece (TP) of the modernized radar. We perform the next required activities:

1. On the TP of the semiconductor transmitter, record the triggers on the Logic analyzer.
2. Put an artificial load of 50 Ω on the 1 MHz output.
3. Redirect triggers to FPGA (ZED board).
4. Generate our signal in the base band (1 MHz) with our sequence of 250 kHz, duration 4 μ S.
5. Perform signal processing in laboratory conditions and try to generate various types of modulation.
6. After completion, play sequences directly on the device measure output power.

The status of the solid-state radar transceiver in the meter range provides at its output a 1 MHz base band transmission pulse at carrier frequencies of 150-170 MHz. On the receiving side, a duplexer with PIN diodes is provided, behind which a low-noise amplifier is installed in the RF range. A module is missing that would lower the modulated signal to the intermediate frequency and/or base band. The shape and modulation of the transmission pulse, as well as the synchronization of the operation of all elements of the radar transceiver with trigger pulses is currently not under our control. In order to overcome the mentioned problems, it is necessary to (in the semiconductor transmitter part):

1. Generate your own trigger pulses - create a functional model on the microcontroller.
2. Generate a modulated signal in the basic range - create a functional model on the microcontroller and DDS signal generator.
3. Perform modulation of the transmission pulse in the basic range to the frequency of the carrier signal - not done.
4. Adjust the voltage and current levels of the generated signal in the RF range for further amplification on the semiconductor transmitter.

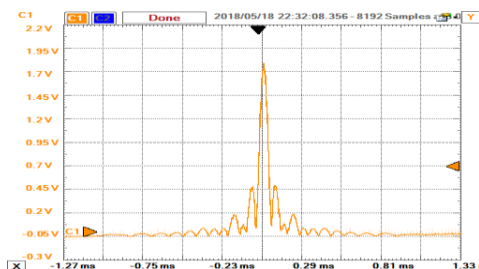
In the semiconductor receiver part, we create a stage of a super heterodyne receiver with an amplifier at intermediate frequency and/or base band in order to

provide the possibility for further digital signal processing and then connect the appropriate hardware assembly for the realization of a digital radar receiver and perform its programming [9].

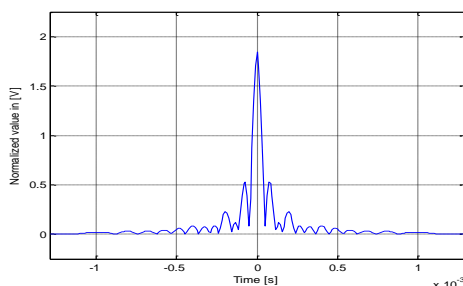
The problematic activities are realizing No.3 in the part of the transmitter and realizing No.1 in the part of the receiver. For the acquisition and digital processing of signals on the basic band of 250 kHz, we have the appropriate hardware components. This base band frequency can provide a resolution cell of at least 600m spatially, which is not by technical requirements, but can be used for testing in the selection of the required parameters. Considering that these are 16-bit A/D converters, as well as a combination of long and short pulse application, the installation of an analog block for Space Time Adaptive Processing (variable gain in reception time) is not necessary.

4.3. Results of matched filtering of radar signals using the FPGA Zedboard

The performance analysis and confirmation of validity of the results obtained using FPGA Zedboard is presented. That will be realized performing comparison between results from the program Matlab, and results which were obtained using FPGA Zedboard, using instrument Analog Discovery in oscilloscope mode. On the output we expected a series of absolute values of autocorrelation peaks. In order to highlight the shape of autocorrelations on the output, it will be presented an enlarged picture of one autocorrelation. On the Pic. 6 and 7 it was displayed autocorrelations of LFM sequence with 25 elements.



Picture 6. The autocorrelation of LFM sequence obtained using FPGA Zedboard



Picture 7. The autocorrelation of LFM sequence obtained using program Matlab

5. CONCLUSION

In this paper, we present example of use the FPGA

technology in radar signal processing. Designing from a software architecture perspective, using tools such as integrated development environments, source code revision control and bug tracking, and creating embedded documentation will all greatly enhance project productivity. The FPGA is capable of very high signal processing performance, thus mitigating large data bandwidths and host CPU loads. The technology facilitates very flexible applications: the same hardware can be customized to meet quite different requirements simply by loading the application-specific firmware. Total system costs are reduced by leveraging the use of a single FPGA card among several systems, and by the consolidation of functions from many discrete hardware components onto a single card.

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