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SOFTWARE-DEFINED RADAR DIGITAL EXCITER, RECEIVER, AND SIGNAL PROCESSOR

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Abstract: *We present a software-defined radar digital back-end (DBE) applicable in fully coherent radars with a power amplifier (PA) transmitter. DBE includes a digital exciter (DEX), receiver digital front-end (DFE), and radar signal processor (RSP). DEX performs direct digital synthesis of the transmit waveform and the local oscillator signal, along with synchronization signals. DFE accepts the intermediate-frequency signal and performs digital down-conversion, filtering, and decimation. Pulse compression, Doppler filtering, and constant false alarm rate detection are performed in the RSP. We use a commercial off-the-shelf, high-performance embedded computing platform to implement the DBE, with DEX and DFE implemented on a field-programmable gate array, and RSP implemented on a general-purpose processor. To test the DBE, we connect it with an existing PA-based analog front-end (AFE), antenna sub-system, and radar data processor. Field tests show that DBE enables the function of a fully coherent pulsed air-surveillance radar, capable of continuously tracking a multitude of aircraft, on both short and long distances, while successfully mitigating both clutter and noise interference. Although the field tests are performed only with very high frequency (VHF) band radar hardware, if connected with an appropriate AFE, DBE could be used in radars operating at higher frequencies.*

Keywords: *radar, receiver, signal processing, software defined, waveform synthesis.*

1. INTRODUCTION

Software-defined radar (SDR), with exciter, receiver, and signal processor realized digitally on reconfigurable hardware, is an established design approach with numerous implementations on commercial off-the-shelf (COTS) hardware [1]. This paper concerns the digital back-end (DBE) of such a radar, comprising: (1) a digital exciter (DEX) for direct digital synthesis (DDS) of the transmit waveform, local-oscillator (LO) signal, and trigger signals; (2) a receiver digital front-end (DFE) that digitizes the intermediate frequency (IF) echo and performs digital down-conversion (DDC), filtering, and decimation; and (3) a radar signal processor (RSP) for pulse compression (PC), Doppler filtering (DF), and detection. In a complete radar, the DBE operates with an

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analog front-end (AFE) encompassing a power amplifier (PA) transmitter, and a radar data processor (RDP) for plot extraction and tracking.

Radars of this class transmit through a solid-state PA, whose modest peak power (commercial units reach the order of kilowatts [2]) is compensated by long pulses with intrapulse modulation and PC [3], [4]. Practical operation requires interleaving short and long pulses, transmitting at several pulse repetition frequencies (PRF), and suppressing clutter by moving target indication (MTI) or moving target detector (MTD) processing [3].

Reported SDR systems largely fall into two categories. General-purpose frameworks like GNU Radio with USRP-class hardware are used to build experimental processing chains, but operate at low power and short range, e.g., detecting a 0.1 m² drone out to about 150 m [5]. At the other end, dedicated DBEs implementing the full pulse-Doppler chain (DDC, PC, MTD, and constant-false-alarm-rate (CFAR) detection) have been realized on custom field-programmable gate array (FPGA) boards for specific radars [6]. The DBE described here occupies a different point in the SDR space: it is built on a COTS high-performance embedded computing (HPEC) platform, partitioning the DEX and DFE onto an FPGA and the RSP onto a general-purpose processor (GPP), aiming at applicability in fully coherent PA-based radars.

The contributions of this paper are the following: (1) an integrated, COTS-based radar DBE that combines the DEX, DFE, and RSP; (2) a hardware/software partitioning that maps the DEX and DFE functions onto an FPGA and the RSP onto a GPP; (3) support for complex waveforms, including interleaved short and long pulses and multiple PRFs, together with MTI or MTD clutter suppression; (4) a demonstration that the DBE, combined with a PA-based AFE and an antenna, constitutes a functioning fully coherent very high frequency (VHF) air-surveillance radar, validated in the field against live air traffic, with applicability to higher frequency bands given a suitable AFE.

2. REQUIREMENTS AND CONSTRAINTS

The operating concept from Section 1 imposes the following requirements on the DBE:

- it shall provide fully coherent operation;
- it shall operate in real time;
- the transmit waveform shall support configurable intrapulse modulation;
- it shall support interleaving of two pulses, short and long, the short pulse restoring the short-range coverage lost to eclipsing during the long pulse [3];
- the carrier frequency, the pulse duration, and the pulse repetition interval (PRI) shall be configurable;
- it shall support pulse-to-pulse carrier-frequency and PRI agility;
- it shall mitigate clutter and noise interference, with multiple-PRF operation used to circumvent the effects of the blind Doppler intervals introduced by clutter suppression [3].

3. SYSTEM ARCHITECTURE

The DBE comprises three logically distinct subsystems: DEX, DFE, and RSP. The DEX and DFE execute as deterministic hardware pipelines on the FPGA, while the RSP runs as software on the GPP. Both processing domains are hosted on a single COTS HPEC platform, which provides the shared backplane, deterministic synchronization, and high-bandwidth data transport.

The block diagram of DBE is shown in Figure 1. The transmit signal flows from the DEX through a digital-to-analog (D/A) converter to the AFE for power amplification. The DEX generates triggers that coordinate the AFE transmit/receive switch and signal the start of reception. Echo returns are collected by the antenna sub-system, amplified and down-converted by the AFE to the analog IF (AIF), and presented to the DFE for digitization. The DFE extracts the complex envelope and applies decimation. The decimated complex envelope samples are organized into frames, together with the azimuth value at the moment of the originating pulse transmission and pulse metadata. Frames are transferred from the FPGA to GPP memory via direct memory access (DMA) and delivered to the RSP through a callback interface. After processing, the RSP produces a real-valued radar video signal, framed with azimuth, and passes it to an external RDP for downstream plot extraction and tracking [3, Fig. 1.2].

The DBE's COTS HPEC platform is based on the NI FlexRIO system. It comprises a transceiver module providing analog-to-digital (A/D) and D/A conversion, an FPGA module, a real-time controller based on a GPP, and a shared chassis. FlexRIO modules have been employed in radar applications before [7].

The partitioning of the DBE follows the principle: sample-synchronous processing on the FPGA, frame-based processing on the GPP. The DEX and DFE form streaming, sample-synchronous pipelines with strict latency bounds. The RSP's algorithms are compute-intensive but tolerate the latency of frame assembly, and benefit from the numerical precision and vectorization capabilities of a modern GPP, the flexibility of software reconfiguration and the easier integration with RDP.

4. SUBSYSTEM DESIGN

4.1. Digital Exciter (DEX)

The DEX is built on the DDS principle [4, Ch. 6]. Its block diagram is shown in Figure 2. The transmit waveform is defined as a pre-computed complex envelope of a pulse, stored in FPGA memory. The pulse duration and all intrapulse modulation parameters of the waveform are set from the configuration transferred from the GPP. The complex envelope is up-sampled by an interpolation chain comprising a multiplierless cascaded integrator-comb (CIC) filter, followed by a finite impulse response (FIR) filter that compensates the CIC amplitude response and provides precise anti-imaging filtering [8]. Then, the complex envelope is translated to the digital IF (DIF) by complex multiplication with a complex sinusoid from a

numerically controlled oscillator (NCO). The DIF is configurable, allowing the carrier frequency to be adjusted. The digital complex pulse at the DIF is interpolated to the output sampling rate by a digital interpolator inside the D/A converter on-board the transceiver module. The D/A converter then applies a digital complex modulator to up-convert the signal from the DIF to the carrier frequency. The I component of the resulting signal is D/A-converted, and the output is cleaned by on-board and external analog low-pass filters.

The LO signal is synthesized independently as a complex sinusoid at a fixed DIF value by a separate NCO on the FPGA. The output is interpolated, up-converted, and D/A-converted through a separate D/A channel on the transceiver module, producing the analog sinusoid that drives the AFE's analog down-conversion mixer. Both the waveform DIF mixer and the LO NCO operate within the same FPGA clock domain. The per-pulse phase reset of both NCOs ensures that each transmitted pulse has a well-defined, repeatable phase relationship with the LO, which is required for coherent reception and DF.

The trigger pulses that mark the instant of each pulse transmission are output from the FPGA through the transceiver's digital I/O lines. Triggers are derived from the same FPGA clock that drives waveform synthesis. Trigger timing and DIF are configurable per-pulse from a preset sequence transferred from the GPP.

4.2. Receiver Digital Front-End (DFE)

The DFE (Figure 3) comprises three stages: (1) A/D conversion of the AIF echo signal; (2) DDC from the AIF to the complex baseband; and (3) a filtering and decimation chain that reduces the sampling rate while providing spectral selectivity. The A/D conversion is performed on the transceiver module, while the DDC and decimation execute on the FPGA.

The AIF signal is digitized by the A/D converter of the transceiver module. Collection of the converted samples is synchronized with the trigger routed from the DEX.

The complex envelope of the digitized real-valued AIF signal is extracted by complex mixing with a digital complex sinusoid [8]. The sinusoid is generated by an NCO set to the AIF, with its initial phase reset on each trigger edge (essential for coherence across pulses).

The complex envelope is decimated using a cascaded pair of FIR decimators, each performing low-pass filtering followed by down-sampling by an integer factor [8].

Assembled complex envelope frames are written to a first-in-first-out buffer on the FPGA, from which they are read by the GPP via DMA and delivered to the RSP.

4.3. Radar Signal Processor (RSP)

The RSP processing chain (Figure 4) comprises five stages: (1) PC; (2) DF; (3) envelope detection; (4) CFAR detection; and (5) frame combining. These stages are applied sequentially, with the DF stage being the only point of branching between MTI and MTD modes.

PC resolves targets in range by matched filtering the received echo against the transmitted pulse template. It is implemented via multiplication in the discrete Fourier transform (DFT) domain [3]. A Taylor window is applied to the matched-filter coefficients for sidelobe control.

To suppress clutter, DF is performed along the slow-time axis (across successive pulses at each range gate), with two modes available. The first mode is MTI [3], implemented as a FIR filter, with configurable order, applied only within a configurable range window.

As an alternative, MTD processor [3], [9] is available. It transforms a coherent processing interval (CPI)-length sequence of complex input frames into a Doppler-resolved output via two parallel channels. The zero-velocity channel retains near-DC returns: a low-pass integrator accumulates energy across the CPI, followed by magnitude computation and an adaptive range-azimuth clutter map update via exponential averaging. The clutter map based detector compares the magnitudes against the learned clutter levels to produce a detection mask for the zero-Doppler bin. The non-zero Doppler channels begin with a high-pass FIR filter. A Taylor-windowed DFT bank then resolves returns across Doppler frequency for all range gates simultaneously. After magnitude computation per Doppler channel, a sliding-window cell-averaging CFAR (CA-CFAR) [3] detector is applied in the range domain. The outputs of all channels pass through a pulse-width discriminator and a primitive observation extractor, followed by binary M-of-N integration across successive CPIs. The video synthesizer constructs complex output frames from the observations, making MTD a drop-in replacement for MTI.

After DF, envelope detection converts the complex-valued signal to a real-valued magnitude.

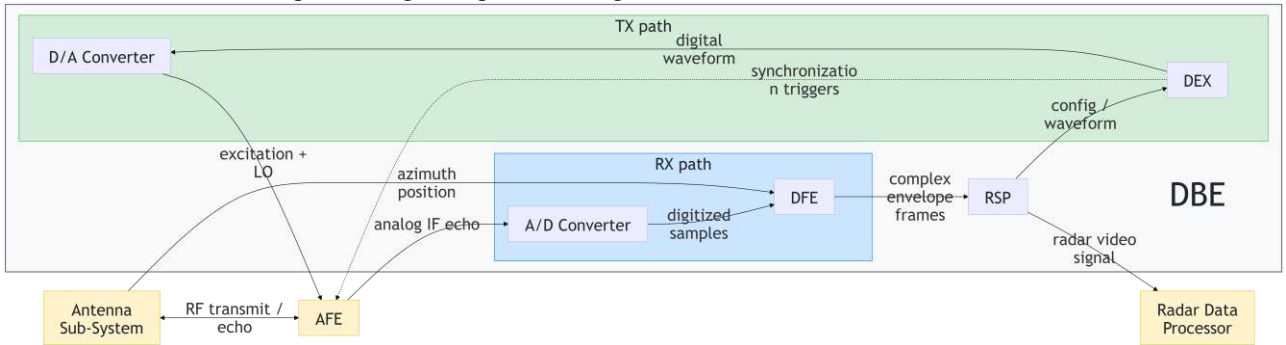


Figure 1. Top-level block diagram: antenna sub-system — AFE — DBE (DEX / DFE / RSP) — RDP.

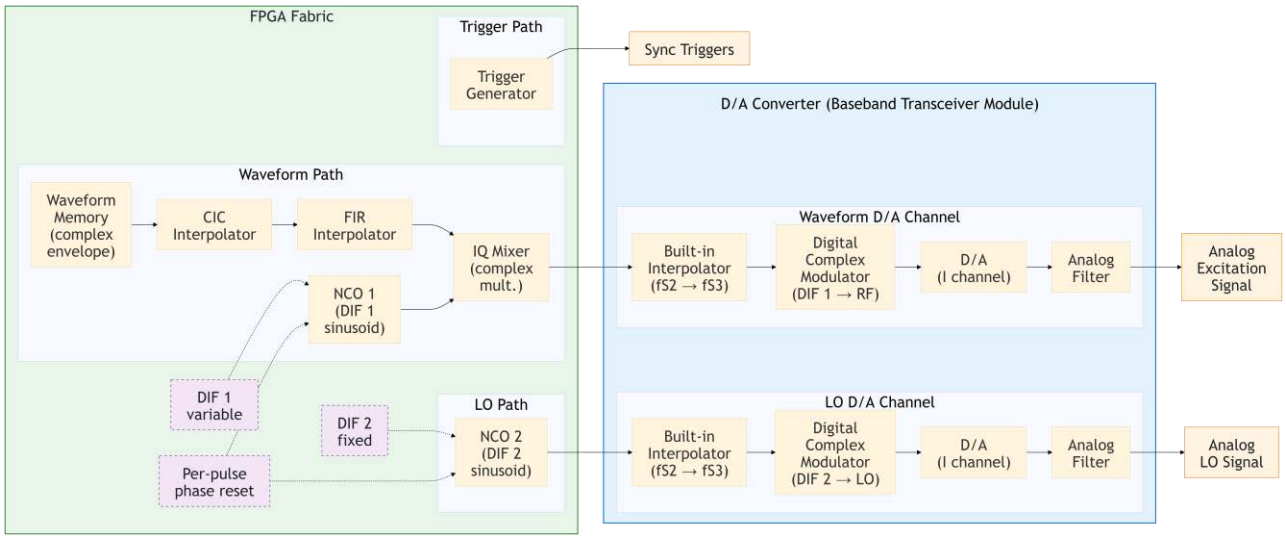


Figure 2. Block diagram of the digital exciter (DEX).

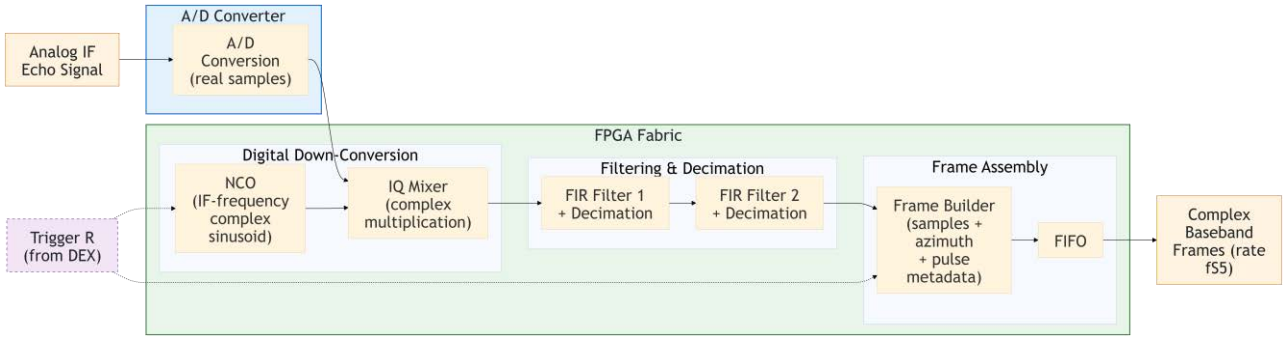


Figure 3. Signal chain of the receiver digital front-end (DFE).

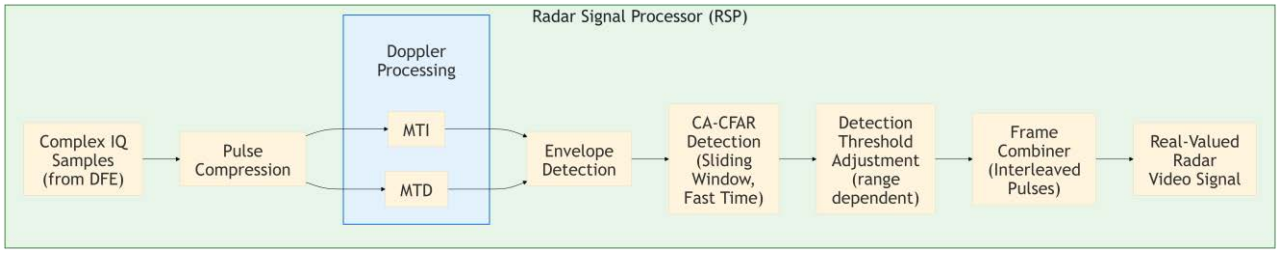


Figure 4. Radar signal processor (RSP) processing chain.

The CFAR detector computes an adaptive threshold from the local noise-plus-clutter environment using a sliding window along the fast-time (range) axis. When the MTI path is active, the detector uses CA-CFAR, with configurable window width, guard-cell count, CFAR constant, and bias. When the MTD path is active, the outer detection stage is bypassed, since the MTD already performs CFAR detection. An optional detection threshold adjustment provides range-dependent scaling of the threshold.

The frame combiner is active only in the interleaved short-and-long-pulse mode. It concatenates the near-range samples from the short-pulse output and the far-range samples from the long-pulse output. The final output is a real-valued radar video signal, accompanied by the azimuth value at transmission time.

5. FIELD TEST AND RESULTS

The DBE was integrated with an existing PA-based AFE, a rotating antenna subsystem designed for VHF-band operation, and a RDP running on a GPP. The RDP comprises a plot extractor [10], a tracker [11], and a radar display application that visualizes radar video, tracks, and annotation overlays [12].

Evaluation was carried out using two complementary operational modes. In live field mode, the DBE was connected directly to the AFE and antenna, with echo signals from real airborne targets digitized and processed in real time. The complex envelope data entering the RSP was recorded digitally by the RSP. In replay mode, recorded data is injected into the same data entry path used by live hardware, ensuring the same input signal and processing pipeline as in the live field mode.

From the available field recordings, four situational windows were selected for evaluation. These “scenarios” were opportunistic observations captured from live air traffic during the recording sessions. After preliminary analysis, stationary clutter fields were mapped by correlating radar returns with terrain data. To prevent the

formation of tracks on dense clutter returns, a circular forbidden track-initiation zone was configured around the radar site. The four scenarios are described below.

The objective of scenario 1 was to demonstrate sustained tracking of a large number of simultaneous airborne targets. Figure 5 shows the result. Continuous tracks are maintained across the surveillance volume, confirming that the DBE's processing pipeline supports simultaneous tracking of multiple targets under realistic clutter conditions. The result demonstrates that the DBE, when combined with the antenna sub-system, the AFE and the RDP, satisfies the requirement for air-surveillance operation over a wide coverage area.

Scenario 2 compared MTI and MTD processing in the context of tracking far-range targets. The recorded signal was re-processed with two different configurations: MTI and MTD, both evaluated against the same set of targets. Figure 6 presents the two processing variants side by side. In both MTI (top) and MTD (bottom) configurations, the far-range target at ~245 km is tracked successfully. Both processing variants are capable of tracking targets at long range on this dataset, demonstrating operational flexibility in the choice of DF strategy.

The 3rd scenario evaluated tracking performance at short range, where the eclipsing caused by long-pulse transmission can leave a blind zone if not compensated. As shown in Figure 7, targets at 9 km (blue) and 15 km (yellow) are tracked consistently. Critically, the interleaved short pulse restores coverage in the near-range zone that would otherwise be eclipsed [13].

The 4th scenario quantified the impact of DF on track quality when targets traverse a clutter field originating from a known mountain. The tracks of three targets passing through the clutter field were evaluated under three processing configurations: no DF, MTI, and MTD (Figure 8). In the left panel (no DF), strong clutter returns generate numerous false detections. Multiple spurious tracks appear in the clutter field, and the legitimate track histories for two of the three targets are corrupted by clutter-induced detections. In the center panel (MTI), the stationary clutter is suppressed, and the target tracks are clean and continuous. In the right panel (MTD), the target tracks are similarly clean and continuous. The before-and-after comparison shows that both MTI and MTD achieve an adequate level of clutter suppression on this dataset.

6. CONCLUSION

This paper presented a SDR DBE that integrates a DEX, a DFE, and a RSP on a COTS HPEC platform. The DEX and DFE were mapped to a FPGA as deterministic, sample-synchronous hardware pipelines, while the RSP runs as software on a GPP. This FPGA/GPP partitioning exploits the complementary strengths of each domain.

The DEX employs DDS with CIC + FIR interpolation and per-pulse NCO phase reset to guarantee full coherence across the pulse train. The DFE performs DDC and two-stage FIR decimation. The RSP chains frequency-domain PC, DF (either MTI or MTD), envelope detection, and CFAR detection into a single configurable pipeline.

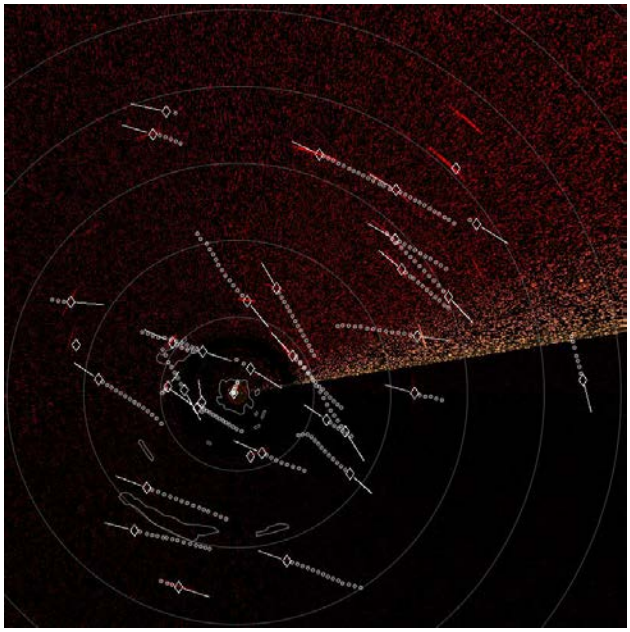


Figure 5. Multi-target tracking. Radar video (red), tracks (white), clutter fields (gray polygons).

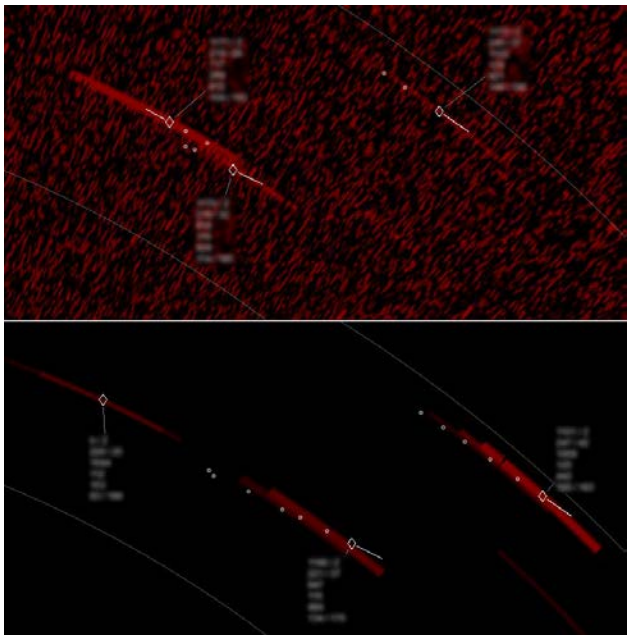


Figure 6. Far-range tracking — MTI (top) versus MTD (bottom). Radar video (red), tracks (white).

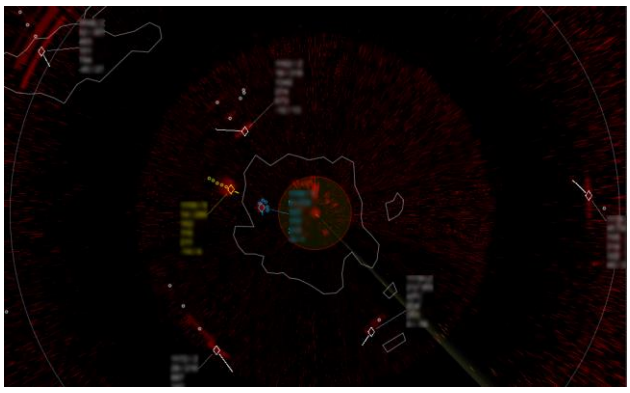


Figure 7. Near-range tracking. Radar video (red), tracks (color-coded), clutter fields (gray polygons).

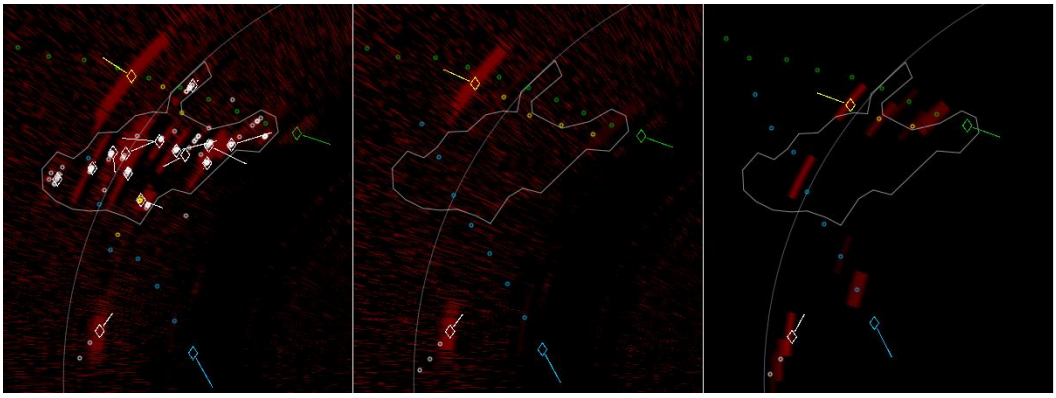


Figure 8. Clutter-field tracking — Doppler filtering disabled (left), MTI (center), MTD (right). Radar video (red), tracks (color-coded), clutter field (gray polygon).

The DBE supports complex waveforms including interleaved short and long pulses, and pulse-to-pulse carrier-frequency and PRI agility.

Field tests against live air traffic, carried out with the DBE integrated into a proof-of-concept PA-based VHF air-surveillance radar, demonstrated continuous tracking of multiple simultaneous airborne targets across the wide area, including far-range target at ~245 km and near-range target at ~9 km. Both MTI and MTD processors were shown to provide effective clutter mitigation.

Although validated with VHF-band hardware, the DBE's signal-processing architecture is frequency-agnostic. Given an appropriate AFE and antenna sub-system, the same DEX, DFE, and RSP pipeline can be applied to radars operating at higher frequency bands, consistent with the system's software-defined design philosophy.

Future work could include deploying the DBE in higher frequency bands to validate its scalability, extending the RSP with additional CFAR and Doppler-processing algorithms, and extending the RSP's interface to RDP.

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